THIN FILM PROCESS

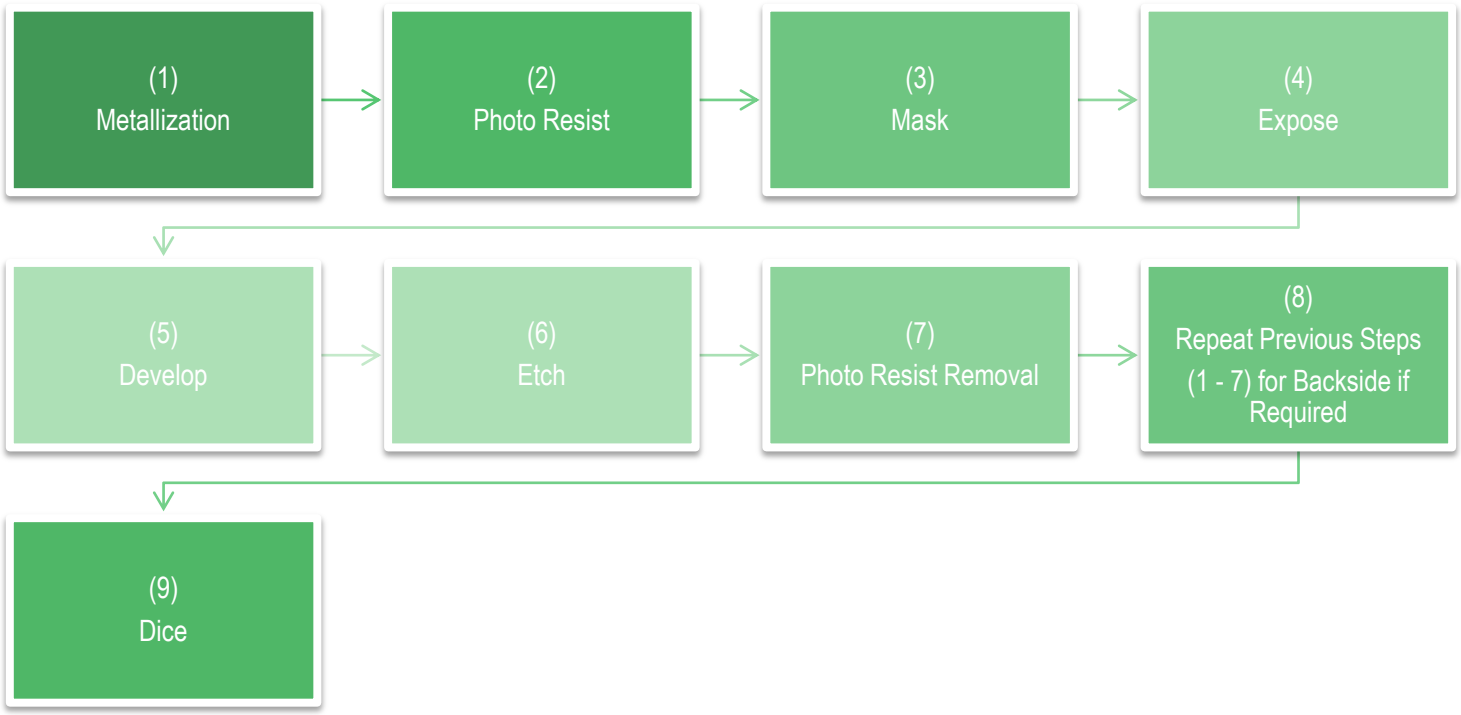

Figure 1: Basic thin film processing.

- Thin Film Processing
  - A resistive layer is sputter before the metallization, if required.
  - Circuits with resist layer will require an additional mask.
  - When processing resistors, steps 2 – 7 (Figure 1) are repeated again after step 7 in order to remove the metallization and expose the resist layer. (See Figure 2).
  - For pre-drilled substrates, the vias are filled during the metallization process.
  - Vias are filled from both sides.

THIN FILM DESIGN GUIDELINES

FOR CHIP AND SMT COMPONENTS 2011-01-27

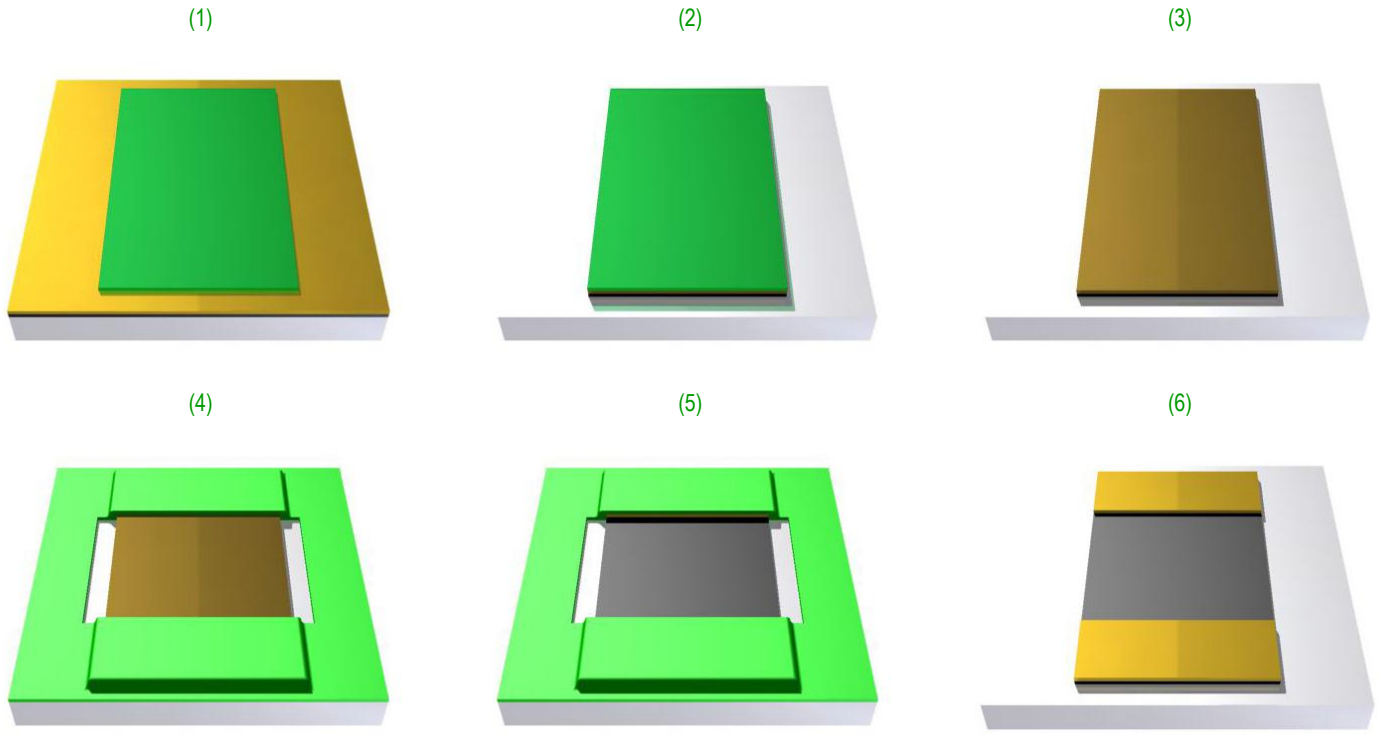

Figure 2: Resistor processing illustration. The first mask will define the composite pattern (1). Etching will remove the composite metalliation (2). First photoresist is removed (3). A second mask will define the resistor dimension; notice that the resist exposure area is oversize to ensure that all the metallization is removed (4). The metal will be etched away leaving the resistor (5). The photoresist is then removed leaving the desired circuit (6).

GUIDELINES

- CAD Drawings
  - Define layers for related objects i.e. conductor, resists, via, chip, polyimide, solder.
  - CAD drawing should be drawn in inches (with an aspect ratio of 1:1).
  - The lower left chip corner is defined as the datum.
  - Objects should be closed polylines.
  - One polyline defining the outer perimeter of an object, i.e., no additional lines (or polyline objects) crossing other lines (or polyline objects).
  - Use a rectangle to define the chip perimeter; fiducials are not required.
  - Leave 0.005 pull-back from edge to minimize jagged metals edges after dice.

- Vias
  - Via Holes should be 1:1 (ratio of via diameter to substrate thickness).
  - Via Hole ratio of 3:4 is possible for special applications.
  - Via Hole must have a pad (circular or square) and must be double the via diameter.
  - Via Pad can be 3:2 (ratio of via pad diameter to via hole diameter), however, the yield will decrease.
  - For Via Pad of 3:2 or smaller, a filled via can improve the yield but at an increased cost.
  - For wrap around vias, the dicing pull-back is 0.002".

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- Resistors
  - Standard Resistivity: 50 and 100 Ω/□
  - Special Resistivity: 20 to 200 Ω/□ (increased cost)
  - Resistor Tolerance (Bake): ±10% or ±5% (reduced yields)
  - Resistor Tolerance (Laser Trimmed): ±1% or ±0.5% (reduced yields)
  - Minimum Resistor Dimension: 0.001

- Manufacturing Tolerance
  - Smallest Feature: 0.0005 line and spaces
  - Feature Tolerance: ±0.0001 (special); ±0.0002 (typical)
  - Dice Tolerance: ±0.002 (typical)
  - Via hole location tolerance: ± 0.002 (relative to datum)
  - Via diameter tolerance: ± 0.001 (typical) on front side
  - Via diameter from front-to-back: 10% reduction

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